GUJARAT TECHNOLOGICAL UNIVERSITY

Bachelor of Engineering
Subject Code: 3172420
Semester – VII

Subject Name: **FPGA in Power Electronics Applications**

Type of course: Professional Elective Course

Prerequisite: 1. Analog & Digital Circuits **(**3142408)
2. Microcontrollers Architecture, Interfacing and Applications (3152409)

Rationale: In today's digital era, every real-life system has become digital. Every industrial application has some digital system inside it. Hence, it becomes important to understand the digital system design for every electrical and electronics engineering student. In case of Power Electronics, real time control of the system can not be achieved without involving programmable system. There are many situations coming in front of designer where he need to choose appropriate tool among DSP, microcontroller and FPGA. This subject focuses on FPGA and VHDL. Hence, designer can select appropriate programmable devices from available devices.

Teaching and Examination Scheme:

Teaching Scheme			Credits	Examination Marks				Total Marks
L	T	P	C	Theory Marks		Practical Marks		
				ESE (E)	PA (M)	ESE (V)	PA (I)	
3	0	2	4	70	30	30	20	150

Content:

Sr. No.	Course Content	Total Hrs.
1	Introduction: Revision of digital electronics, Boolean algebra, minimization of functions, gates, combinational logic, flip-flop, registers, timing, counter circuits, CMOS circuits Digital system design, Microprocessor basics, computer architecture basics.	6
2	Digital System Design: Design and analysis of synchronous sequential circuits, top- down design, controller design, state diagram, Finite state machines, synchronization	8
3	VHDL introduction: Entity, architecture, operators, Concurrency, data flow and behavioral modeling, structural model, simulation, classes, data types, concurrent statements, sequential statements, loops, modelling flip flops, registers, sequential circuit synthesis, Library and packages, operators, delay modeling etc.	8
4	VHDL Programming and Digital System Design: VHDL coding, Coding of a simple FSM, Test bench, Digital system design using VHDL	8
5	Programmable Logic Devices: Evolution of PLD, Simple PLD, PLD fitting, Complex PLD, PROM, PAL, PLA, Examples of PLD and CPLD ICs	5
6	Field Programmable Gate Array: FPGA introduction, internal block diagram, CLB (Configurable logic block) or LAB (Logic array block), LUT (Look Up Table), FPGA from Xilinx, Altera, Actel etc., Concept of routing in FPGA	8
7	Programmable Logic Devices in Power Electronics Applications: Use of PLDA for generating control signals for power electronics applications.	2

Suggested Specification table with Marks (Theory): (For BE only)

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Distribution of Theory Marks					
R Level	U Level	A Level	N Level	E Level	C Level
20	**30**	**15**	**20**	**10**	**05**

Legends: R: Remembrance; U: Understanding; A: Application, N: Analyze and E: Evaluate C: Create and above Levels (Revised Bloom's Taxonomy)

Note: This specification table shall be treated as a general guideline for students and teachers. The actual distribution of marks in the question paper may vary slightly from above table.

Reference Books:

1. Embedded System Design A Unified Hardware Software Introduction, Frank Vahid, Tony Givargis, Wiley India
2. FPGA based system design, Wayne Wolf, Pearson
3. A VHDL Primer, J Bhaskar, Pearson
4. A Verilog HDL Primer, J Bhaskar
5. A VHDL Synthesis Primer, J. Bhaskar

Course Outcome:

After learning this course, the students should be able:

Sr. No.	CO statement After learning this course, the students should be able to	Marks % weightage
CO1	understand concepts of digital system design	25
CO2	understand concepts of Hardware Description Language	25
CO3	identify appropriate Programmable Logic Device for given application	25
CO4	design small practical application using HDL	25

The following are suggested list of experiments based on theme:

1. Study of Design flow for digital logic design using HDL
2. Study of VHDL
3. Study of the simulator for VHDL (eg. Model Sim, GHDL, Xilinx Vivado, etc.)
4. To model and simulate simple combinational circuits.
5. To model and simulate a 1 bit full adder and 4 bit parallel adder.
6. To model and test simple sequential circuit (e.g. binary up/down counter) using FSM (Mealy / Moore)
7. To model and simulate memory
8. To model and simulate a single purpose processor. (This is having weightage of 3 experiments. This experiment should be given in group of 2-3 students. Each group should be assigned a separate single purpose processor. The examples are watch dog timer, PWM, 7 segment display controller, key board interface, GCD, binary multiplier etc.).

Major Equipment: Computer/VHDL simulator

List of Open-Source Software/learning website:

1. https://nptel.ac.in/courses/117/108/117108040/#
2. https://www.coursera.org/learn/fpga-hardware-description-languages
3. https://www.mooc-list.com/course/hardware-description-languages-fpga-design-coursera